#1. Which combination of two of the following is fastest/most efficient for large data transfers.

- Programmed I/O
- Interrupt-driven _________________________ / _________________________
- DMA
- CPU blocked (Polling)

#2. The MMU translates ____________ to ____________ addresses.

The ____________ caches these recently translated addresses.

#3. A _________________ cache ensures the data in the cache is the same as what is in main memory.

#4. Paging and swapping refer to parts of or entire program images being moved back and forth between what 2 storage areas/hierarchies?

_____________ and _______________

A ____________ occurs because a page is needed but was not found to be in main memory.

#5. This type of I/O uses regular instructions to perform I/O and not any special instructions.

____________________________________

#6. List the 5 basic C Runtime sections in order from low memory to high memory for the SPARC architecture:

_____________ (low memory)
_____________
_____________
_____________
_____________ (high memory)

(over)
What question would you most like to see on the Final Exam?